ISSN: 2277-9655
Impact Factor: 4.116
CODEN: IJESS7

IJESRT
INTERNATIONAL JOURNAL OF ENGINEERING SCIENCES & RESEARCH TECHNOLOGY

MAGNETIC TUNNEL JUNCTION MODEL BASED UNIVERSAL NAND AND NOR LOGIC GATES

Joyanto Roy Choudhary*, Sumitesh Majumder, T K Maiti

DOI: 10.5281/zenodo.802807

ABSTRACT

We have presented here magnetic tunnel junction (MTJ) model based universal NAND and NOR logic gates and studied the proposed universal gates by both experimental and simulation methods. Experimental results substantiates with both the simulated and theoretical results.

INTRODUCTION

Magnetic Tunnel Junction (MTJ) device is presently a very promising device because of its mesmerizing physics, their non-volatility, reconfigurable capability, fast-switching speed, small-dimension, CMOS compatibility, and also its different applications areas like spintronics logic devices and circuits, magnetic storage devices, magnetic sensors and communication etc. Recently, researchers have been established the MTJ based different logic gates [1-6] and in these developed logic gates, MTJs have used as main devices for logical computations and intrinsically enable logic-in-memory architectures with no need for extra hardware. In a logic mode the MTJs act as the basic elements for computations and in a memory mode they are used for non-volatile storage purposes. This enables for the expanding of non-volatile electronics from memory to logical computing applications without any sensing amplifiers and intermediate circuitry as compared to the hybrid CMOS based non-volatile logic circuits. MTJ is a spintronic device which gives a spin orientation in two opposite direction - one parallel and another anti-parallel (shown in Fig.1) i.e. MTJ behaves as a resistor with two resistance characteristics (high and low) depending on the direction of magnetization in the two ferromagnetic layers. Electrically this resembles with diode behavior with high current in the forward direction and low current in the reverse direction.

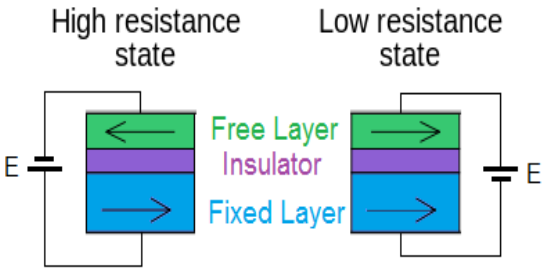


Fig.1: MTJ with high and low resistance state

Here we have exploited the above-mentioned properties to realize the universal NAND and NOR logic gates [7] with a simple behavioral model of MTJ device (shown in Fig. 2) which has been represented as two identical diodes with a low resistance (R_P) during parallel magnetization and high resistance (R_{AP}) during anti-parallel magnetization.

ISSN: 2277-9655
Impact Factor: 4.116
CODEN: IJESS7

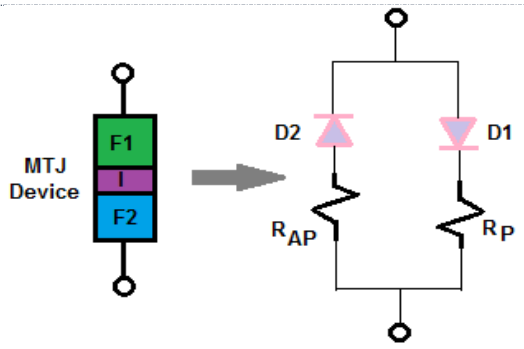


Fig.2: Magnetic Tunnel Junction device model

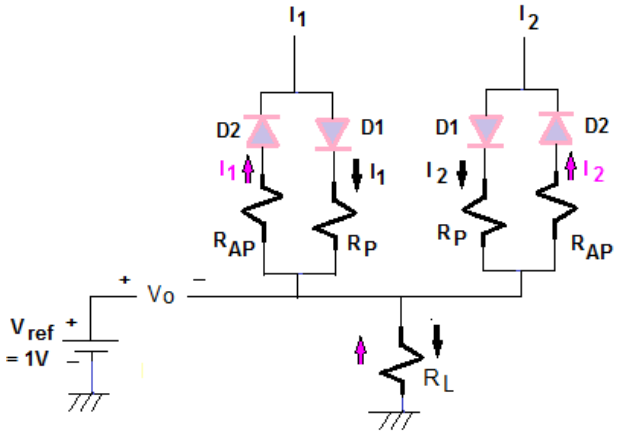
THEORY

The proposed MTJ model based NAND and NOR gates have been shown in Fig. 3a and Fig. 3b, respectively. For both the the bidirectional current sources (I_1 and I_2), we have developed two opamp (OP07) based voltage to current converter (VIC) [8] with MTJ model as grounded load which is shown in Fig. 4. When the input currents are positive values, the currents (I_1 & I_2) (flow directions have shown with black colored arrow) flow in the path containg R_L, R_P and diode D_1. The resistances R_P resemble the low resistance during the parallel magnetization for both MTJs and When the input currents are negative values, the currents (I_1 & I_2) (flow directions have shown with pink colored arrow) flow in the path containg R_L, R_{AP} and diode D_2. The resistances R_{AP} resemble the high resistance during the anti-parallel magnetization for both MTJs.

For VIC with grounded load (Fig.4), the currents (I_1 & I_2) can be expressed as

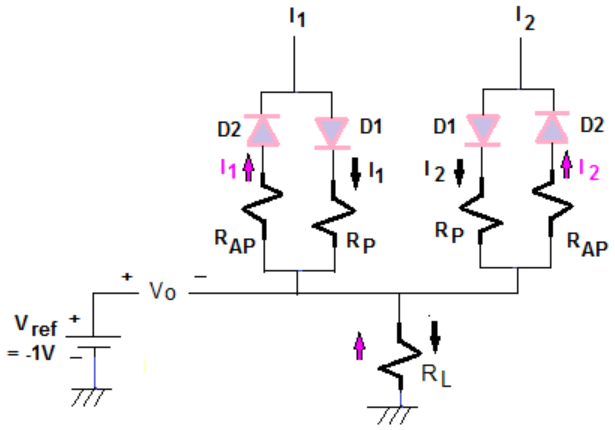
$$I_1 = \frac{V_1}{R} \text{.....(1)} \;\&\; I_2 = \frac{V_2}{R} \text{.....(2)}$$

The currents I_1 and I_2 will be either positive or negative depending on the polarity of voltages V_1 and V_2.



a)

ISSN: 2277-9655
Impact Factor: 4.116
CODEN: IJESS7



b)

Fig. 3: MTJ model based 2-input a) NAND and b) NOR gate

The operation of NAND logic gate (Fig. 3a) is explained as follows: when the input currents I_1 = -1.021mA (logic '0') and I_2 = -1.021mA (logic '0'), the output voltage can be written as

$$V_0(00) = V_{ref} - (-I_1 - I_2)R_L \quad \ldots\ldots(3)$$

where $V_O(00)$ is the circuit output voltage when I_1 = -1.021mA (logic '0'), I_2 = -1.021mA (logic '0') and V_{ref} = +1.000V, the reference voltage.

Similarly, the output voltages are:

when I_1 = -1.021mA (logic '0'), I_2 = +1.021mA (logic '1')

$$V_0(01) = V_{ref} - (-I_1 + I_2)R_L \quad \ldots\ldots(4)$$

when I_1 = +1.021mA (logic '1'), I_2 = -1.021mA (logic '0')

$$V_0(10) = V_{ref} - (I_1 - I_2)R_L \quad \ldots\ldots(5)$$

when I_1 = +1.021mA (logic '1'), I_2 = +1.021mA (logic '1')

$$V_0(11) = V_{ref} - (I_1 + I_2)R_L \quad \ldots\ldots(6)$$

The operation of NOR logic gate (Fig. 3b) is same as the operation of NAND logic gate (Fig. 3a) even the equations (Eqn.3 to Eqn.6) are also same except the value of V_{ref} which is -1.000V.

Since we have taken the diode pairs from the transistor array of IC LM389 (Make: Texas Instrument) [9], we have considered here the diodes are identical in all respects i.e. $V_{D1} = V_{D2} = V_D$

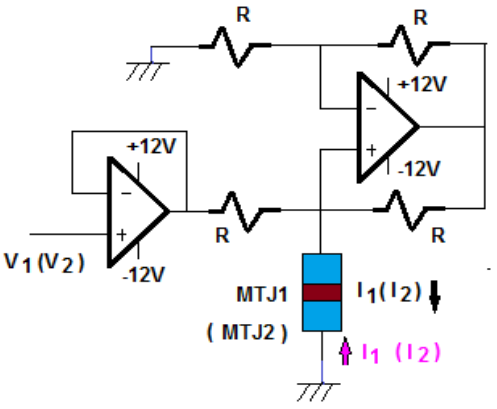


Fig. 4: Opamp based Voltage to current converter [8] with MTJ as grounded load

Equation (3) to equation (6) signify that when input voltages are positive, the forward currents follow the the low resistance (R_P) paths and when input voltages are negative, the reverse currents follow the the high resistance (R_{AP}) paths. It is very obvious that the above output voltage equations are independent of diode voltage (V_D) and hence these parameters are independent of ambient temperature effect also as diode voltage varies with ambient temperature.

ISSN: 2277-9655
Impact Factor: 4.116
CODEN: IJESS7

RESULTS AND DISCUSSIONS

We have exploited the circuit of Fig.3 for both simulation study using sophisticated Multisim software (Make: National Instrument; Version 11.0) and experimental of the proposed MTJ model based universal logic gates. For both the experimental and simulation studies, we have taken opamp (OP07), $V_1 = V_2 = \pm 4.7V$ and $V_{ref} = +1.000V$ (-1.000V) for NAND (NOR) gate, $R = 4.603k\Omega$, $R_P = 0.567k\Omega$, $R_{AP} = 1.467k\Omega$ and $R_L = 0.977k\Omega$. The experimental, simulated and theoretical results have tabulated in the Table 1 and Table 2 for 2-input NAND and NOR gate. Table 3 shows the corresponding logical current inputs and voltage outputs assuming for input currents, -1.021mA = logic '0 and +1.021mA = logic '1' and for output voltages, negative voltage = logic '0 and positive voltage = logic '1'. This is obvious from the Tables that the experimental results agree with the simulated and theoretical results and satisfy the truth table [7] of the conventional universal logic gates.

Table 1: Experimental, Simulation and Theoretical results
for 2-input NAND logic gate
$R = 4.603k\Omega$, $R_P = 0.567k\Omega$, $R_{AP} = 1.467k\Omega$ and $R_L = 0.977k\Omega$.
$V_1 = V_2 = \pm 4.7V$ and $V_{ref} = +1.000V$

Input currents (mA)		Output voltage (V_O) (Volts)		
I_1	I_2	Experimental	Simulation	Theoretical (Eqn.3-Eqn.6)
-1.021	-1.021	+3.050	+2.993	+2.955
-1.021	+1.021	+1.052	+1.000	+1.000
+1.021	-1.021	+1.026	+1.000	+1.000
+1.021	+1.021	-1.013	-0.993	-0.995

Table 2: Experimental, Simulation and Theoretical results
for 2-input NOR logic gate
$R = 4.603k\Omega$, $R_P = 0.567k\Omega$, $R_{AP} = 1.467k\Omega$ and $R_L = 0.977k\Omega$.
$V_1 = V_2 = \pm 4.7V$ and $V_{ref} = -1.000V$

Input currents (mA)		Output voltage (V_O) (Volts)		
I_1	I_2	Experimental	Simulation	Theoretical (Eqn.3-Eqn.6)
-1.021	-1.021	+1.023	+0.993	+0.995
-1.021	+1.021	-1.043	-1.000	-1.000
+1.021	-1.021	-1.054	-1.000	-1.000
+1.021	+1.021	-3.042	-2.993	-2.995

Table 3: Logical Current Inputs and Voltage Outputs for 2 input NAND and NOR gates using Table -1 and Table -2

For input currents, -1.021mA = logic '0 and +1.021mA = logic '1'
For output voltages, (-) ve voltage = logic '0 and (+) ve voltage = logic '1'

Logical Current Inputs		Logical Voltage Outputs		
I_1	I_2	Experimental	Simulation	Theoretical (From Eqn.3-Eqn.6)

ISSN: 2277-9655
Impact Factor: 4.116
CODEN: IJESS7

		NAND	NOR	NAND	NOR	NAND	NOR
0	0	1	1	1	1	1	1
0	1	1	0	1	0	1	0
1	0	1	0	1	0	1	0
1	1	0	0	0	0	0	0

CONCLUSION

This research paper focuses mainly on the study and realization of MTJ model based NAND and NOR logic gates and their truth table verifications. The experimental results show excellent agreement with the simulated and theoretical results. The study also fulfill the truth table of the conventional universal NAND and NOR logic gate s.

Joyanto Roychoudhary (Department of Electronics and Communication Engineering, Neotia Institute of Technology Management and Science, West Bengal, India)

Sumitesh Majumder (Department of Applied Electronics and Instrumentation Engineering, Netaji Subhash Engineering College, Techno City, Garia, Kolkata – 700 152, West Bengal, India)

T K Maiti (Professor and Head of the department of Applied Electronics and Instrumentation Engineering, Netaji Subhash Engineering College, Techno City, Garia, Kolkata – 700 152, West Bengal, India)

REFERENCES

[1] J. Wang, H. Meng, and J.-P. Wang (2005), "Programmable spintronics logic device based on a magnetic tunnel junction element," *J. Appl. Phys.*, vol. 97, no. 10, p.10D509.
[2] Sankha S. mukherjee, Santosh K. Kurinec (2009), 'A stable spice macro-model for magnetic tunnel junctions for applications in memory and logic circuits', IEEE transactions on Magnetics, vol. 45, no. 9, pp.3260-3268
[3] A. Lyle, J. Harms, S. Patil, X. Yao, D. Lilja, and J. P. Wang, (2010),"Direct Communication Between Magnetic Tunnel Junctions for Nonvolatile Logic Fan-out Architecture," Appl. Phys. Lett., vol. 97, no.23, p. 152504
[4] Y. Gang, W. Zhao, J. O. Klein, C. Chappert, and P. Mazoyer, (2011), "A High-Reliability, Low-Power Magnetic Full Adder," IEEE Trans. Magn., vol. 47, no.11, pp. 4611–4616.
[5] A. Lyle, S. Patil, J. Harms, B. Glass, X. Yao, D. Lilja, and J. P. Wang, (2011),"Magnetic Tunnel Junction Logic Architecture for Realization of Simultaneous Computation and Communication," IEEE Trans. Magn., vol. 47, no. 10, pp.2970–2973.
[6] H. Mahmoudi, T. Windbacher, V. Sverdlov, and S. Selberherr, (2013), "Implication Logic Gates using Spin-Transfer-Torque-Operated Magnetic Tunnel Junctions for Intrinsic Logic-in-Memory," Solid-State Electron., vol. 84,pp. 191–197.
[7] Albert P. Malvino and Donald P. Leach, Digital Principles and Applications, 4th Edition, TMH Publishing Co. Ltd., New Delhi, India 2008.
[8] Sergio Franco, Design with Operational Amplifiers & Analog Integrated Circuits, 3rd Edition, McGraw Hill Education, 2014.
[9] LM389 Low Voltage Audio Power Amplifier with NPN Transistor Array, National Semiconductor, December 1994 (www.engineering.uiowa.edu/sites/default/files/ees/files/NI/pdfs/00/78/DS007847.pdf)

CITE AN ARTICLE

Choudhary, J. R., Majumder, S., Dr, & Maiti, T. K. (2017). MAGNETIC TUNNEL JUNCTION MODEL BASED UNIVERSAL NAND AND NOR LOGIC GATES. *INTERNATIONAL JOURNAL OF ENGINEERING SCIENCES & RESEARCH TECHNOLOGY*, *6*(6), 38-45. doi:10.5281/zenodo.802807